Abstract of the Disclosure

A serial peripheral interface apparatus has a second parallel write buffer to load in a subsequent data byte while a current data byte is being transferred serially through the apparatus instead of waiting for the previous data byte to complete the serial transfer and other commands to avoid write collision. The subsequent data byte is transferred into the second parallel write buffer only after the software driven CPU examines the status of a load enable and the status of a write buffer provided by a finite state machine controller. The software driven CPU orders the subsequent data byte to be transferred into the second parallel write buffer when the load enable is favorable and the second parallel write buffer is available. The load enable becomes favorable when a bit counter counts the first half of the transfer of the previous data set. Thus, the second parallel write buffer avoids the stretching the master clock and improves data throughput of the system.